CLAIMS

1. A circuit protected against transient disturbances, including a combinatory logic circuit (10) having at least one output (A), characterized in that it includes:

a circuit (20, 11) for generating an error control code for said output; and

a memory element (24, 24') arranged at said output, controlled by the control code generation circuit to be transparent when the control code is correct, and to keep its state when the control code is incorrect.

2. The protected circuit of claim 1, characterized in that the error control code generation circuit includes a circuit (20) for calculating a parity bit (P) for said output (A) and a circuit (22) for checking the parity of the output and of the parity bit.

3. The protected circuit of claim 1, characterized in that the error control code generation circuit includes a duplicated logic circuit (11), said memory element (24') being provided to be transparent when the outputs of the logic circuit (10) and of the duplicated circuit (11) are identical, and to keep its state when said outputs are different.

4. The protected circuit of claim 1, characterized in that the error control code generation circuit includes an element (90) for delaying said output by a predetermined duration greater than the maximum duration of transient errors, said memory element (24') being provided to be transparent when the outputs of the logic circuit and of the delay element are identical, and to keep its state when said outputs are different.

5. The protected circuit of claim 3, characterized in that said memory element (24') is formed from a logic gate providing said output of the logic circuit, this logic gate including at least two first transistors (MN1, MP2) controlled by a signal (a) of the logic circuit and at least two second transistors (MP1, MN2) controlled by the corresponding signal (a*) of the duplicated circuit, each of the second transistors

being connected in series with a respective one of the first transistors.

6. A circuit protected against transient disturbances, including a combinatory logic circuit (10) having at least one output (A) connected to a first synchronization flip-flop (70, 92) rated by a clock (CK), characterized in that it includes a second flip-flop (71, 93) connected to said output and rated by the clock delayed by a predetermined duration (δ), and a circuit (74, 95) for analyzing the outputs of the flip-flops, and in that the analysis circuit (95) indicates an error if the flip-flop outputs are different.

7. The protected circuit of claim 6, characterized in that the second flip-flop (93) is controlled by the same clock as the first flip-flop, but by a different edge or level of this clock.

8. A circuit protected against transient disturbances, including a combinatory logic circuit (10) having at least one output (A) connected to a first synchronization flip-flop (70) rated by a clock (CK), characterized in that it includes a second flip-flop (71) rated by the clock and receiving said output delayed by a predetermined duration (δ), and a circuit (74) for analyzing the flip-flop outputs, and in that the analysis circuit indicates an error if the flip-flop outputs are different.

9. A circuit protected against transient disturbances, including three identical logic circuits (10a, 11a, 10b), characterized in that each of the logic circuits is preceded by a two-input memory element (24a, 24b, 24c) respectively receiving the outputs of the two other logic circuits, each memory element being provided to be transparent when its two inputs are identical, and to keep its state when the two inputs are different.

10. The protected circuit of claim 9, characterized in that the logic circuits are inverters and the memory elements include, in series, two P-channel MOS transistors and two N-channel MOS transistors, a first one of the inputs of the memory

element being connected to the gates of a first one of the P-channel MOS transistors and of a first one of the N-channel MOS transistors, and the second input of the memory element being connected to the gates of the two other transistors.

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